



because the timing illustrated assumes instantaneous switching of the switches so that the switches transition from on to off or off to on instantaneous. As will be noted below with regard to the invention, in practice such switches have timing delays and such timing delays can be problematic if not controlled and/or compensated. In the square wave or six step operation illustrated in Figure 1B, the six electronic switches S1-S6 are turned on every 60° in the proper order to produce a three phase balanced waveform. For example, when switch S1 is commanded ON, its IGBT is gated on ON and the current will flow through the IGBT or through its anti-parallel diode. If the current is positive (into the AC traction motor), then the IGBT of S1 will be conducting. If the current is negative (from the motor), then the anti-parallel diode connected to the IGBT of S1 will conduct. In either case, the switch S1 which is commanded will be conducted.

[0005] Figure 1C illustrates prior art phase commands for pulse width modulated (PWM) operation of the inverter of Figure 1A. PWM is used to vary the power supplied to the AC motor. During PWM operation, the six electronic switches S1-S6 are turned ON and OFF at a much higher switching frequency than the fundamental frequency of ON and OFF operation as illustrated in Figure 1B. In Figure 1C, the exemplary commands that may go to one of the switches is illustrated. The commands provided to its corresponding switch in the same phase would be opposite the commands illustrated in Figure 1C, except for minimum ON/OFF and snubber reset times required. For example, when the top switch S1, S3, S5 is ON, its corresponding bottom switch S4, S6, S2, respectively, is OFF and vice versa. Figure 1C shows firing pulses for a given phase. Other phases are delayed by 120 degrees and 240 degrees.

[0006] Figure 2 illustrates a prior art block diagram of a control logic for a single inverter. The traction motor control logic illustrated in Figure 2 generates the firing commands f4 and f5 to phase A. The frequency and timings are controlled such that the AC motor generates the desired amount of torque. Thus, the control logic varies the flux, frequency, voltage, current etc in the machine. The control logic also functions to protect the traction motor and the traction inverter components. The output of this logic is a three phase command, one to each of the phases A, B and C. When a firing command signal is high, its corresponding top (positive) switch is turned ON and when the signal is low the bottom (negative) switch is turned ON. Signal f1 is the phase A command signal so that Figure 2 illustrates the details of phase A. Phases B and C are similarly configured. The phase A firing command is split into the top and bottom switch command signals f2 and f3. The gate driver/switch receives signals f2 and f3 and the status feedback is sent back to the control logic. Signals f4 and f5 are the status feedback from the top and bottom switches. Operation of phase B and C are similar.

[0007] Figure 3 is a prior art timing diagram of the logic commands. This figure illustrates the timing diagrams of the various signals for phase A described in Figure 2. At time t0, the phase A command signal f1 transitions from 0 to 1 indicating that the top switch of phase A should be ON and the bottom switch should be OFF. Since previously the bottom switch was ON, the first event is at t1 where switch command signal f3 (which is the command to the bottom switch) goes low, commanding the bottom switch to turn OFF. At time t2, the bottom switch turns OFF and the status feedback signal f5 transitions to a low value indicating such turn off. This f5 transition

is detected by the phase A firing command logic which then commands the top switch ON at time t3 as indicated by the switch command signal f2 going high. This occurs after a short period of time to allow any snubber settling time or margin. As a result, the status feedback signal f4 transitions to a high value at t4 indicating the top switch is ON. This completes a 0 to 1 transition of a phase A command signal f1. Similar timings are illustrated in Figure 3 for a transition from 1 to 0. In particular, at t5, the phase A command signal f1 transitions to 0, at t6 the top switch command signal f2 transitions to OFF, at t7 the top switch status feedback signal f4 transitions to OFF, at t8 the bottom switch command signal f3 transitions to ON and at t9 the bottom switch status feedback signal f5 transitions to ON. This complete cycle is repeated again starting at time t10.

[0008] Thus, as illustrated in Figure 1A wherein a single inverter supplies all power to an AC motor, it is apparent that the amount of power supplied to the AC traction motor is controlled by and related to the amount of power that can be supplied through a single switch of each phase of the single inverter. As a result, the total power that can be supplied to the AC traction motor is limited by the power rating or the maximum power that each switch can handle. In order to increase the load bearing capacity of a non-highway vehicle, for example, an off highway vehicle, a freight locomotive or a passenger locomotive, the AC traction motor and the power supply to it must be increased to provide more torque for handling the additional load. This in turn requires an increase in the power handled by each of the switches. Unfortunately, IGBTs or GTOs have a limited power handling capability and the cost of designing and manufacturing higher power

switches can be prohibitive. Therefore, there is a need for an inverter for supplying power to AC traction motors which can handle additional power requirements and which has a reasonable manufacturing and replacement cost. There is also a need for employing similar components in such inverters as the components presently in use in existing non-highway vehicles in order to reduce the inventory necessary to supply spare parts for such vehicles. There is also a need for a multiple inverter configuration for supplying power to traction motors in which the inverters are balance or matched so that the inverters operate with disparity such that one inverter carries significantly more current than the other, which could cause overheating or burnout.

BRIEF DESCRIPTION OF THE INVENTION

[0009] In one form, the invention comprises a circuit for connection to a DC bus for providing power to a traction motor of an non-highway vehicle. A first inverter connects between the DC bus and the traction motor. A second inverter connects between the DC bus and the traction motor. The second inverter is in parallel connection with the first inverter.

[0010] In another form, the invention comprises a non-highway vehicle. An DC power source driven by an engine provides DC power via a DC bus. A circuit connects between a traction motor and the DC bus for providing power to the traction motor. The circuit comprises at least two inventers, a first inverter for connection between the DC bus and the traction motor and a second inverter for connection between the DC bus and the traction motor. The second inverter is in parallel connection with the first

inverter. A controller coordinates operation of the first and second inverters.

[0011] Various other embodiments and separate aspects of the invention will be described below and/or will be immediately apparent to those skilled in the art.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The features of the invention believed to be novel are set forth in the appended claims. The invention, however, together with further objects and advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawings in which:

[0013] Fig. 1A is a schematic diagram of a three phase single inverter according to the prior art for supplying power to an AC motor.

[0014] Fig. 1B is a timing diagram according to the prior art showing the status of the transistors S1-S6 of Fig. 1A.

[0015] Fig. 1C is a timing diagram according to the prior art illustrating phase commands for an exemplary operation of pulse width modulation of each of the transistor S1-S6 of Fig. 1A.

[0016] Fig. 2 is a block diagram of control logic according to the prior art for generating the firing commands controlling the status of switches S1-S6 of Fig. 1A.

[0017] Fig. 3 is a prior art timing diagram of the logic commands f1-f5 employed by the control logic of Fig. 2 when operating according to the prior art.

[0018] Fig. 4 is a schematic diagram of a three phase dual inverter according to the invention for supplying power to an AC motor.

[0019] Fig. 5 is a timing diagram of the logic commands f1-f5 employed by the control logic of Fig. 2 of one phase when operating according to the invention.

[0020] Fig. 6 is a timing diagram illustrating the time delay between the actual turn off event of the negative switches (e.g., switches S4x and S4y as controlled by f5x and f5y at times t2x and t2y, respectively, of Fig. 5). Fig. 6 illustrates the delay related to a negative to positive transition when the direction of current is from the traction motor to the inverter at the time of switching and assumes that the currents (i_{ax} and i_{ay}) in the two inverters are the same.

[0021] Fig. 7 is a timing diagram illustrating the time delay between the actual turn off event of the negative switches (e.g., switches S1x and S1y as controlled by f4x and f4y at times t4x and t4y, respectively, of Fig. 5). Fig. 7 illustrates the delay related to a negative to positive transition when the direction of current is from the inverter to the traction motor at the time of switching and assumes that the currents (i_{ax} and i_{ay}) in the two inverters are the same.

[0022] Fig. 8 is a timing diagram illustrating the time delay between the actual turn off event of the negative switches (e.g., switches S1x and S1y as controlled by f4x and f4y at times t7x and t7y, respectively, of Fig. 5). Fig. 8 illustrates the delay relating to a positive to negative transition when the direction of current is from the traction motor to the inverter at the time of switching and assumes that the currents (i_{ax} and i_{ay}) in the two inverters are the same.

[0023] Fig. 9 is a timing diagram illustrating the time delay between the actual turn off event of the negative switches (e.g., switches S4x and S4y as controlled

by $f5x$ and $f5y$ at times $t9x$ and $t9y$ respectively, of Fig. 5). Fig. 9 illustrates the delay related to a positive to negative transition when the direction of current is from the inverter to the traction motor at the time of switching and assumes that the currents (i_{ax} and i_{ay}) in the two inverters are the same.

[0024] Fig. 10 is a schematic diagram illustrating a three phase dual inverter of the invention for supplying power to an AC motor including impedance devices in each phase.

[0025] Fig. 11 is a schematic diagram of a three phase dual inverter of the invention for supplying power to an AC motor including independent cables connecting each phase component of the inverter to the corresponding phase winding of the traction motor.

[0026] Fig. 12 is a timing diagram of the logic commands $f1-f5$ employed by the control logic of Fig. 2 when operating according to another embodiment of the invention employing a control algorithm to delay switches which operate faster.

[0027] Fig. 13 is a schematic of a logic and a closed loop current equalizing regulator of the invention for delaying switches which operate faster.

[0028] Fig. 14 is a schematic of a logic and a closed loop current equalizing regulator according to another embodiment of the invention for delaying switches which operate faster.

[0029] Fig. 15 is a timing diagram of the logic commands $f1-f5$ employed by the control logic of Fig. 2 when operating according to another embodiment of the invention in which the positive ON event is delayed.

[0030] Fig. 16 is a timing diagram illustrating the differential positive current [Differential current =

(iayt5-iayt0)-(iaxt5-iaxt0)] overlaying the logic commands of Fig. 15.

[0031] Fig. 17 is a timing diagram illustrating the differential negative current [Differential current = (iayt5-iayt0)-(iaxt5-iaxt0)] overlaying the logic commands of Fig. 15.

[0032] Fig. 18 is a timing diagram of the logic commands f1-f5 employed by the control logic of Fig. 2 when operating according to another embodiment of the invention in which the negative OFF event is delayed.

[0033] Fig. 19 is a timing diagram illustrating the differential negative current [Differential current = (iayt5-iayt0)-(iaxt5-iaxt0)] overlaying the logic commands of Fig. 18.

[0034] Fig. 20 is a timing diagram illustrating the differential positive current [Differential current = (iayt5-iayt0)-(iaxt5-iaxt0)] overlaying the logic commands of Fig. 18.

[0035] Fig. 21 is a timing diagram of the logic commands f1-f5 employed by the control logic of Fig. 2 when operating according to another embodiment of the invention in which the positive OFF event is delayed.

[0036] Fig. 22 is a timing diagram illustrating the differential positive current [Differential current = (iayt5-iayt0)-(iaxt5-iaxt0)] overlaying the logic commands of Fig. 21.

[0037] Fig. 23 is a timing diagram illustrating the differential negative current [Differential current = (iayt5-iayt0)-(iaxt5-iaxt0)] overlaying the logic commands of Fig. 21.

[0038] Fig. 24 is a timing diagram of the logic commands f1-f5 employed by the control logic of Fig. 2 when

operating according to another embodiment of the invention in which the negative ON event is delayed.

[0039] Fig. 25 is a timing diagram illustrating the differential positive current [Differential current = $(i_{ayt5} - i_{ayt0}) - (i_{axt5} - i_{axt0})$] overlaying the logic commands of Fig. 24.

[0040] Fig. 26 is a timing diagram illustrating the differential negative current [Differential current = $(i_{ayt5} - i_{ayt0}) - (i_{axt5} - i_{axt0})$] overlaying the logic commands of Fig. 18.

[0041] Fig. 27 is a schematic diagram illustrating the invention for employing current and voltage sensors in the dual inverter of Fig. 10.

[0042] Fig. 28 is a schematic diagram illustrating the invention for employing current and voltage sensors in the dual inverter of Fig. 11.

[0043] Fig. 29 is a schematic diagram illustrating another embodiment according to the invention for employing current and voltage sensors in the dual inverter of Fig. 11.

[0044] Fig. 30 is a schematic diagram illustrating another embodiment according to the invention for employing current and voltage sensors in the dual inverter of Fig. 11.

[0045] Fig. 31 is a timing diagram of the logic commands f1-f5 employed by the control logic of Fig. 2 when operating according to another embodiment of the invention in which the positive ON event is delayed (e.g., Figs. 15 and 16) showing the voltages V_x and V_y .

DETAILED DESCRIPTION OF THE INVENTION

[0046] Figure 4 illustrates an "ideal" or "model" two inverter schematic diagram according to the invention. As

noted above and as will be discussed in greater detail below, this embodiment is referred to as an "ideal" or "model" embodiment because it assumes that all the components are balanced or matched which, in practice, is not frequently attainable or cost effective. In particular, Figure 4 illustrates a first three phase inverter 40x including switches S1x to S6x and a second three phase inverter 40y including switches S1y to S6y. The inverters 40x and 40y are connected in parallel to a DC bus having a positive rail 42 and a negative rail 44. The two inverters 40x and 40y are similar in configuration to the inverter illustrated in Figure 1. Inverters 40x and 40y are operated in parallel to increase the total capacity (e.g., torque, current and/or horsepower) of the power being provided to the AC motor 46. Corresponding switches of the two inverters are turned ON and turned OFF at the same time. For example, switch S1x of inverter 40x is operated simultaneously and in the same state as switch S1y of inverter 40y. Similarly, the other five switches of inverter 40x are operated simultaneously with their corresponding switches of inverter 40y.

[0047] Those skilled in the art will recognize variations to the dual inverter illustrated in Figure 4. For example, although the invention has been described herein as a dual inverter, it is contemplated that the invention may be implemented by two or more inverters and that any of the embodiments of the invention may include three or more inverters. For example, Figure 4 shows a third inverter in phantom, in which case each inverter would be configured and sized to carry one third of the power required by the AC motor 46. Also, although the invention illustrates the inverters in parallel, certain embodiments may employ a series configuration. Also,

although the invention has been illustrated as supplying power to a three phase motor, it is contemplated that it may be used to power any multi-winding motor such a two phase or a six phase motor. For example, for a six phase motor, the first three phases of the motor may be operated 120° apart in synchronism with the last three phases, respectively, or the first three phases may be operated 120° apart and 180° out of synchronism with the last three phases, respectively. In addition, although the inverter has been illustrated as a "model" inverter, other embodiments including embodiments wherein the inverters are balanced or matched, as noted below, fall within the scope of the invention.

[0048] Figure 5 illustrates the timing diagram of the various logic signals for phase A of the inverters 40x and 40y illustrated in Figure 4. At time t_0 , the phase A command signal f_1 transitions from 0 to 1 indicating that the top switches should be ON and the bottom switches should be OFF. Since previously the bottom switches were ON, the first events are at t_{1x} and t_{1y} where switch command signals f_{3x} and f_{3y} (commands to the bottom switches S_{4x} and S_{4y}) go low, commanding the bottom switches to turn OFF. At time t_{2x} and t_{2y} , the bottom switches S_{4x} and S_{4y} turn OFF as indicated by the status feedback signals f_{5x} and f_{5y} transitioning from a high to a low value. When the phase A firing command logic detects that both signals f_{5x} and f_{5y} have transitioned to a low signal, it waits a small amount of time (for any snubber settling time or margin) and commands the top switches S_{1x} and S_{1y} to turn ON at time t_{3x} and t_{3y} as indicated by switch command signals f_{2x} and f_{2y} transitioning from a low value to a high value. As a result, the status feedback signals f_{4x} and f_{4y} transition to a high value at time t_{4x}

and t4y indicating the top switches S1x and S1y are closed or ON. This completes a 0 to 1 transition for the phase A command. Similar timings are illustrated for the transitions from 1 to 0. In particular, at time t5, the motor control logic signal f1 transitions to a 0, at t6x and t6y the top switch command signals f2x and f2y transition to OFF, at time t7x and t7y the top switch feedback status signals f4x and f4y transition to OFF indicating that switches S1x and S1y are open, at time t8x and t8y the bottom switch command signals f3x and f3y transition to ON and at time t9x and t9y the bottom switch feedback status signals f5x and f5y transition to ON indicating that the bottom switches S4x and S4y are closed. This completes one cycle for phase A which begins to repeat again at time t10. The phase B top switch S5x and the phase B bottom switch S2x are operated similarly 120° out of phase or later than the phase A switches, the phase B switches being responsive to the phase B command signal. The phase C top switch S3x and the phase C bottom switch S6x are similarly operated 120° after the phase B switches. Corresponding switches of inverter 40x and 40y are operated simultaneously. Thus, phase A top switches S1x and S1y are operated simultaneously; phase A bottom switches S4x and S4y are operated simultaneously; phase B top switches S5x and S5y are operated simultaneously; phase B bottom switches S2x and S2y are operated simultaneously; phase C top switches S3x and S3y are operated simultaneously and phase C bottom switches S6x and S6y are operated simultaneously.

[0049] In contrast to the single inverter configuration as illustrated in Figure 1A, in which a single switch supplies all power to the AC traction motor, it can be seen that the invention as illustrated in Figure

4 is configured such that two switches simultaneously supply power to the AC traction motor 46. Since the two switches are operating in parallel off the same rails 42 and 44 of the DC bus, each switch can have a power rating which is approximately half the total power to be delivered to the AC induction motor 46. In Figure 1, the power to be provided to the motor is limited by the maximum power rating of the switches. In contrast, according to Figure 4 and the invention, the power to be supplied to the AC traction motor 46 is limited by double the power rating of the switches. Thus, the size of the AC traction motor 46 can effectively be doubled since it can be provided with twice the power without a need for an increase in the sizing of the components. For example, according to the prior art, IGBTs have a nominal operating range of 0-2500v and 0-2400A and have a preferred maximum operating limit of 1500v and 2000A. According to the prior art, AC induction motors operating with such IGBTs generally operate at a torque range of 11,000lbft, a current range of 1000ARMS (amperes RMS), and a horsepower rating of 1500. In order to increase these parameters of the AC induction motor, larger rated components would be required. In contrast, according to the invention, such IGBTs can be used in combination with a motor having a current operating range of 2000ARMS, a torque operating range of 22,000lbft, and a horsepower rating of 3000. (Note: these are only examples of operating ranges and amounts.)

[0050] Another aspect of the invention is that the components S1x-S6x and S1y-S6y of the dual inverters illustrated in Figure 4 are the same as the components S1-S6 of the single three phase inverter illustrated in Figure 1A. Thus, additional inventory is not needed to supply the switches of the dual inverter according to the invention as

compared to the switches of the single inverter according to the prior art since both inverters employ the same switching components. Another aspect of the invention is that it provides a fail-safe configuration. For example, if one of the switches of one of the dual inverters fails in an open state, operation of the motor is still possible since the other inverter can supply half power (or more) to the motor.

[0051] Figure 6 illustrates the current waveform for current flowing into the inverter when a negative to positive transition of a switch occurs. In this illustration, the negative switch turn off would effectively control the current. Figure 6 shows the effect of the time delay between the actual turn off of the negative switches (e.g., the turn off of switches S4x, S6x and S2x at t2x and the turn off of switches S4y, S6y and S2y at t2y per Figure 5). Figure 6 assumes that the direction of current is from the load to the inverter at the time of the transition of the switches and further assumes that the current in the two inverters, i.e., the phase A current i_{ax} in inverter 40x and the phase A current i_{ay} in inverter 40y) are the same.

[0052] At time t2x, switch S4x of inverter 40x turns OFF. The current in inverter 40x will switch to the freewheeling path of switch S1x. The total load current remains relatively constant due to the large load inductance. The current levels in the two inverters will differ since S1x and S4y are conducting. The rate at which the currents diverge depends on primarily the inductance in this path. At time t2y, the switch S4y also turns off and the current will be flowing through the freewheeling path of S1x and S1y. If the inductance to each of the inverters is the same, then the slope of the currents will be the

same. So any current difference between the two inverters will remain essentially the same. The difference will die down based on the L/R value. After repeated switching events, the current differences will tend to keep increasing.

[0053] Figure 7 illustrates the current waveform when current is flowing out of the inverter during a negative to positive transition of the switches. Figure 7 illustrates the effects of the time delay between the actual turn off of the negative switches when the direction of current is to the load from the inverter at the time of turn off. At the time of turn off, the current is flowing through the freewheeling diodes so that the commands to turn off devices S4x and S4y have no effect. However, at time t4y, when switch S1y turns on, the current iay flowing through S1y will increase and the current iax flowing through the freewheeling diode of S1x will decrease. Once switch S1x also turns on, the currents will rise at an equal rate.

[0054] Figure 8 is similar to Figure 6 and illustrates the current waveform when current is flowing out of the inverter during a transition from positive to negative of a switch. Figure 9 is similar to Figure 7 and illustrates the current waveform when current is flowing into the inverter during a positive to negative transition of a switch.

[0055] Thus, as can be seen by reviewing Figures 6-9, current differences develop between the currents flowing through the switches in the dual inverters because of a number of factors including varying impedance and varying timing. In order to reduce the current difference or disparity, it is contemplated that one or more devices such as a resistance, or reactance (e.g., inductance or capacitance) or any other impedance devices may be located

in series with each phase to provide a reactance which matches or balances the inverters. Thus, as illustrated in Figure 10, the two inverter schematic diagram includes a reactance R_{xa} in phase A of the inverter 40x and includes a reactance R_{ya} in phase A of the inverter 40y. Similarly, phases B and C include reactances R_{xb} , R_{yb} , R_{xc} and R_{yc} . These reactances in each phase limit the rate of change of current difference and the resistance of the reactants brings the current difference back to zero after each switching cycle. However, such reactances can be costly and require considerable packaging and cooling effort.

[0056] Figure 11 illustrates another preferred aspect of the invention in which independent wiring is used to interconnect the dual inverters with the AC traction motor. In particular, the AC traction motor 46 includes terminals T_a , T_b and T_c on or in close proximity to the motor 46 for receiving the energizing power for phases A, B and C, respectively, for energizing the separate windings of the motor 46. A cable C_{xa} interconnects phase A of inverter 40x with motor terminal T_a . A cable C_{xb} connects the switches of phase B of inverter 40x with motor terminal T_b . A cable C_{xc} connects the switches of phase C of inverter 40x with motor terminal T_c . Similarly, separate cables C_{ya} , C_{yb} and C_{yc} connect phases A, B and C of inverter 40y with motor terminals T_a , T_b and T_c , respectively. These cables will carry half the current from each motor 46. Because of their length and geometry, these cables offer some inductance and resistance. As compared to the reactants approach illustrated in Figure 10, these cables provide much less cost and/or do not necessarily require cooling or other packaging issues. Typically, there is some distance (e.g., 20-100 feet or more) between the motor (which is frequently located under the platform/truck) and

the inverter (which is frequently located over the platform/deck).

[0057] In another embodiment according to the invention, it is contemplated that the controller which controls the switches of the inverters may employ an optimizing algorithm to vary the timing of the transition of the switches. Figure 12 illustrates a timing diagram according to the invention wherein the timing of the switches is optimized. In general, this timing arrangement delays the commands to the switches which operate faster. The faster switches can be determined by empirical data, by specification data, by relative location to other switches, by other information such as actual testing on a circuit-by-circuit basis or by sensing the voltage and/or current and/or status feedback. The purpose of delaying the faster switches is to control any current differences between the two inverters. For example, transitions t_{1x} and t_{1y} which are the switch command signals f_{3x} and f_{3y} for the upper and lower switches, respectively, occur at different times compared to the timing as illustrated in Figure 5. Table 1 shows the control logic for the optimized timing diagram according to Figure 12. In this logic, for every switching point depending on current polarity, there is one switch which can be controlled to balance/match the current.

[0058] Figure 13 illustrates another embodiment according to the invention in which switching delays are determined by control logic which is part of a closed loop regulator (gain control). In particular, the difference between the currents i_{ax} and i_{ay} is determined by a summer 5 or other component and provided to a regulator for determining a delay compensation based on a differential. A closed loop regulator 130 monitors the delay compensation signal as well as other parameters of the system such as

current, voltage and/or temperature. The regulator 130 has a table or algorithm which defines an optimum delay as a function of the monitored parameters. As illustrated in Figure 13, delay is illustrated as a function of current and voltage. Other parameters may be temperature, lot (silicon property, manufacturer, gate drive characteristics/type), etc. The regulator 130 determines the adjustment to the delay compensation signal according to the present current and voltage of the system and provides this to an inverter which then provides a corresponding signal to a mixer M for adjusting the delay compensation signal. Thus, the current error is used to computer delay compensation. The regulator 130 normalizes the delay to the current using an algorithm, function generator or look-up table based on the device characteristics and on certain characteristics. The mixed signal from mixer M including delay compensation is applied to the appropriate switch according to the logic illustrated in Table 1.

Table 1 . Control Logic

Conditions	Action	Don't Care	Comments
Current Positive $ i_x > i_y $	Positive Switch Control Delay turn OFF y positive Delay turn ON of x positive	Negative Switch Control	Need to sample current at twice switching freq to select
Current Negative $ i_x > i_y $	Negative Switch Control Delay turn OFF x negative Delay turn ON of y negative	Positive Switch Control	Need to sample current at twice switching freq to select

[0059] It is contemplated that three such compensation systems may be employed, one for each of the upper switches of one of the inverters. Alternatively, six compensation systems according to Figure 13 may be employed, one for each of the six switches for one of the inverters. Alternatively, twelve (12) compensation systems according to Figure 13 may be employed, one for each edge, current polarity and phase.

[0060] Figure 14 illustrates another embodiment for implementing the current regulator. In Figure 14 the current error is normalized first based on the device and/or circuit characteristics. In particular, depending on the current and/or voltage (and/or temperature) as detected by a regulator (gain control) 40 and depending on the program or table used therein, a first nominal delay signal is provided to an x/y adjustment of the current differential. The output of this block gives a percentage/fractional delay needed to correct the current. This adjusted differential current is provided to the regulator which produces a second delay signal which is then accumulated by a feedback loop. The output of this block which represents percentage/fractional delay correction is converted to the real delay time required by

the gain equalization look up based on current operating conditions.

[0061] Figure 15 illustrates a timing diagram wherein one positive switch has a delay during turn ON transition. All other switchings are assumed to be ideal. ON transitions are delayed. Figure 16 (see modified figure) illustrates a timing diagram corresponding to Figure 15 for positive current whereas Figure 17 (see modified figure) illustrates a timing diagram for negative current. Figure 16 shows the current i_{ax} and i_{ay} . If currents are sampled at t_0 and t_5 (2 samples per switching), at t_5 the differential current due to switching delays during t_0 to t_5 time is given by the difference in the change of current in x during t_0 to t_5 and the change in current in y during t_0 to t_5 . In other words, $\text{diff current} = (i_{ayt5} - i_{ayt0}) - (i_{axt5} - i_{axt0})$. This differential current can be used to compensate the delay in the appropriate switch based on the polarity of the current. In figure 17 it shows that no compensation is necessary for the negative current case. Similarly, Figure 18 illustrates a preferred embodiment of a timing diagram for a negative OFF delay and Figures 19(see modified figure) and 20 (see modified figure) illustrate the timing diagram for negative current and positive current. Figure 21 illustrates a timing diagram for a positive OFF delay and Figures 22 (see modified figure) and 23 (see modified figure) illustrates a timing diagram for positive and negative current. Figure 24 illustrates a timing diagram for negative ON delay and Figures 25 (see modified figure) and 26 (see modified figure) illustrate a timing diagram for positive and negative current. If currents are sampled 4 times a switching cycle, for example at t_0 , t_3 , t_5 and t_8 , then differential current could directly determine which switch

and which edge need to be controlled. It should be noted that the currents could also be different due to conduction loss differences as well as switching time differences. The overall current difference due to conduction loss difference is also compensated by adjusting the switching times. Typically, the conduction loss differences are small.

[0062] Table 2 illustrates one preferred embodiment of the control selection logic according to the invention using 2 samples per switching cycle. Table 3 shows the logic for 4 samplings per switching cycle.

Table 2. Control Delay Selection Logic

Switch	Switch Delay Edge	Current Polarity	Differential current / Edge	Control for twice sampling (at t0 and t5)
Positive	ON	Positive	Positive to Negative Command Transition	Delay + ON switch with positive differential current
Positive	ON	Negative	No count	
Positive	OFF	Positive	Negative to Positive Command Transition	Delay + OFF switch with negative differential current
Positive	OFF	Negative	No count	
Negative	ON	Positive	No count	
Negative	ON	Negative	Negative to Positive Command Transition	Delay - ON switch with negative differential current
Negative	OFF	Positive	No count	
Negative	OFF	Negative	Positive to Negative Command Transition	Delay - OFF switch with positive differential current

Table 3. Control Delay Selection Logic for 4 samples per switching cycle

Differential current interval	Control Delay Edge
T0/t1 to t3	Delay t1
T3 to t5	Delay t3
T5/t6 to t8	Delay t6
T8 to t10	Delay t8

[0063] Figure 27 illustrates the current and voltage sensors used for the two inverter configuration with reactants as illustrated in Figure 10. Current sensors i_{ax} , i_{ay} , i_{bx} , i_{by} , i_{cx} and i_{cy} are used to control motor torque and for differential current control. Voltage sensors v_a , v_b and v_c are used to control motor torque. Alternatively, Figures 28, 29 and 30 illustrate three embodiments for positioning current sensors and voltage sensors in a two inverter system according to the invention with independent wires as illustrated in Figure 11. These current and voltage sensors are used to provide inputs to the regulators 130 and 140 of Figures 13 and 14, respectively. In figure 28, lumped inductors have been removed and cable impedance is depended upon. Figure 29 uses two (motor) current sensors and six voltage sensors v_{ax} , v_{ay} , v_{bx} , v_{by} , v_{cx} and v_{cy} . The sensors v_{ax} and v_{ay} are averaged for motor torque control and the differential voltage is used to control the balance/match current. Figure 30 uses 6 voltage and 6 current sensors. This provides all degrees of freedom for control and diagnostics. If conduction loss differences are ignored, it is possible to compensated with voltage sensors like v_{ax} and v_{ay} without using independent current sensors (for example, see the sensing scheme used in fig 29). In this case the exact switching interval can be obtained from the voltage sensors. Figure 31 shows the voltage for the case shown in figure 16. V_y will go from 0 to full dc voltage first and V_x will change after the

delay. The voltage delay can be determined and used to compensate the appropriate (leading or trailing) edge. For example, if the voltage transition happens during t_3 to t_5 , then t_3 's edge needs to be controlled whereas if the voltage transition happens between t_0 and t_3 , then t_1 's edge need to be controlled. The differential volt seconds may also be used to compensate the timings.

[0064] This invention solves the longstanding problem of expanding the capacity of non-highway vehicles at a reasonably low cost and without the need for high cost inverter components. This invention also solves the longstanding problem of need for a reasonably low cost inverter system for higher power motors in which the inverter system includes low cost, off the shelf components.

[0065] When introducing elements of the present invention or the embodiment(s) thereof, the articles "a," "an," "the," and "said" are intended to mean that there are one or more of the elements. The terms "comprising," "including," and "having" are intended to be inclusive and mean that there may be additional elements other than the listed elements.

[0066] While various embodiments of the present invention have been illustrated and described, it will be appreciated to those skilled in the art that many changes and modifications may be made thereunto without departing from the spirit and scope of the invention. As various changes could be made in the above constructions without departing from the scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.